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SYRIAN PRIVATE UNIVERSITY

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Logic Circuits

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Chapter_ 7

Sequential Logic Circuits Analysis

(تحليل الدارات المنطقية التتابعية)

Lecture _10

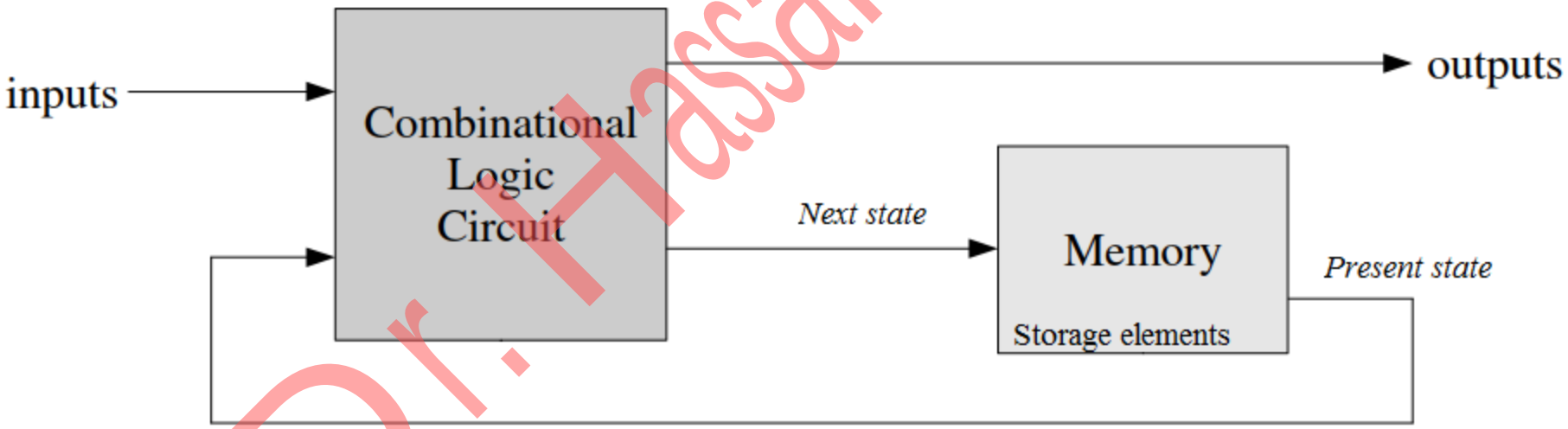
Latches & Flip-Flops

Sequential Logic Circuits (SLC)

- A sequential circuit is a logic circuit whose output(s) is a function of its input(s) and also its internal state(s).
  - The (internal) state of a sequential logic circuit is either a logic 0 or a logic 1, and because of its ability to maintain (الاحتفاظ) a state, it is also called a **memory circuit**.
- The output of a sequential logic circuit is dependent not only on the present inputs, but also on the past sequence of the inputs.
- A sequential logic circuit must "remember" the past history of the inputs.
- It does this using basic memory elements.
  - ✓ Latches
  - ✓ Flip-Flops

Sequential logic circuit architecture

- The block diagram of a sequential circuit, formed by interconnecting (التوصيل المشترك) a combinational circuit and storage elements.
  - ✓ The **storage elements** are circuits that are capable of storing binary information, that will define the **state** of the sequential circuit at that time.
  - ✓ The inputs, together with the present state of the storage elements, determine the binary value of the outputs.



10-1. Latches (الماسكات)

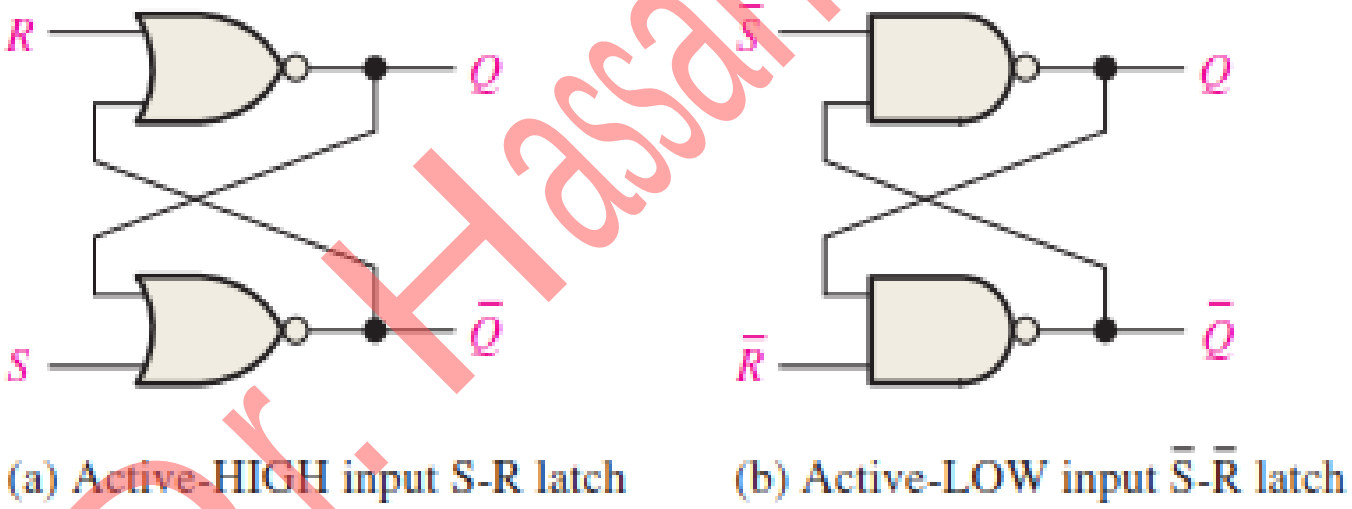
- A **latch** is a temporary (مؤقت) storage device that has **two stable states** (**bistable, ثنائي الاستقرار**).
- It is a basic form of memory.

Types

1. S-R (SET-RESET) Latch
2. Gated S-R Latch
3. Gated D Latch

1. The S-R (SET-RESET) Latch

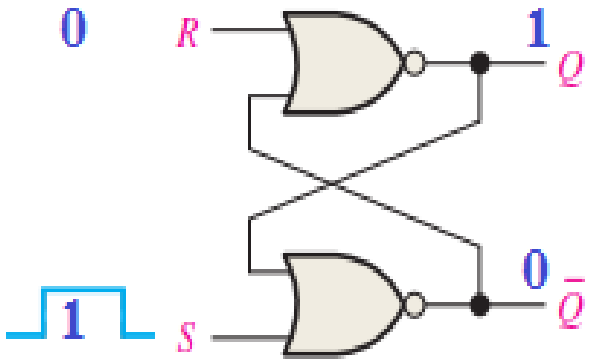
- The **S-R (Set-Reset) latch** is the most basic type.
- It can be constructed from NOR gates or NAND gates.
  - With NOR gates, the latch responds to active-HIGH inputs;
  - With NAND gates, it responds to active-LOW inputs.



(a) Active-HIGH input S-R latch (b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

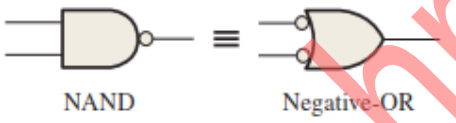
a) The **active-HIGH *S*-*R* latch** is in a stable (latched) condition when both inputs are LOW.

- ***Q*** –is the normal output (المخرج الطبيعي); $\overline{Q}$ -is the complement output.
- Assume the latch is **initially RESET** (***Q* = 0**) and the inputs are at their inactive level (**0**).
- To **SET** the latch (*Q* = 1), a momentary HIGH signal is applied to the ***S*** input while the ***R*** remains LOW.
- To **RESET** the latch (*Q* = 0), a momentary HIGH signal is applied to the ***R*** input while the ***S*** remains LOW.



b) An **active-LOW input** $\overline{S}-\overline{R}$ latch is formed with two cross-coupled **NAND gates**.

- This latch is redrawn with the **negative-OR** equivalent symbols used for the **NAND** gates.



(A negative-OR operation: output is HIGH when either input A or input B is LOW, or when both A and B are LOW)

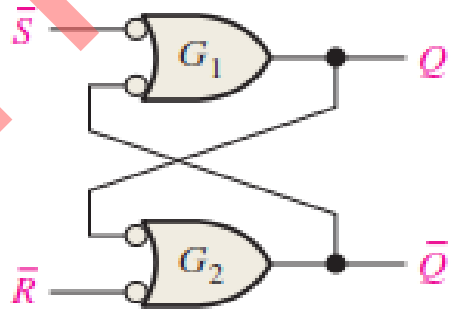
- This is done because LOWs on the *S* and *R* lines are the activating inputs.

- Let's start by assuming that both inputs and the *Q* output are HIGH, which is the **normal latched state**.
- Since the *Q* output is connected back to an input of gate G_2, and the $\overline{R}$ input is HIGH, the output of G_2 must be LOW. This LOW output is coupled back to an input of gate G_1, ensuring (ضمان) that its output is HIGH.

The SET state

When the Q output is HIGH, the latch is in the **SET** state.

- Q output will remain in this state until a LOW is applied to the $\overline{R}$ input.
- With LOW on $\overline{R}$ input and HIGH on $\overline{S}$ input, the output of gate G_2 is forced HIGH.
- This HIGH on the $\overline{Q}$ output is coupled back to an input of G_1, and since the $\overline{S}$ input is HIGH, the output of G_1 goes LOW.
- This LOW on the Q output is then coupled back to an input of G_2, ensuring that the $\overline{Q}$ output remains HIGH even when the LOW on the $\overline{R}$ input is removed.



The RESET state

- When the *Q* output is LOW, the latch is in the **RESET** state.
  - The latch remains in the RESET state until a LOW is applied to the $\overline{S}$ input.
- In normal operation, the outputs of a latch are always complements of each other.

❖ **When *Q* is HIGH, $\overline{Q}$ is LOW, and when *Q* is LOW, $\overline{Q}$ is HIGH.**

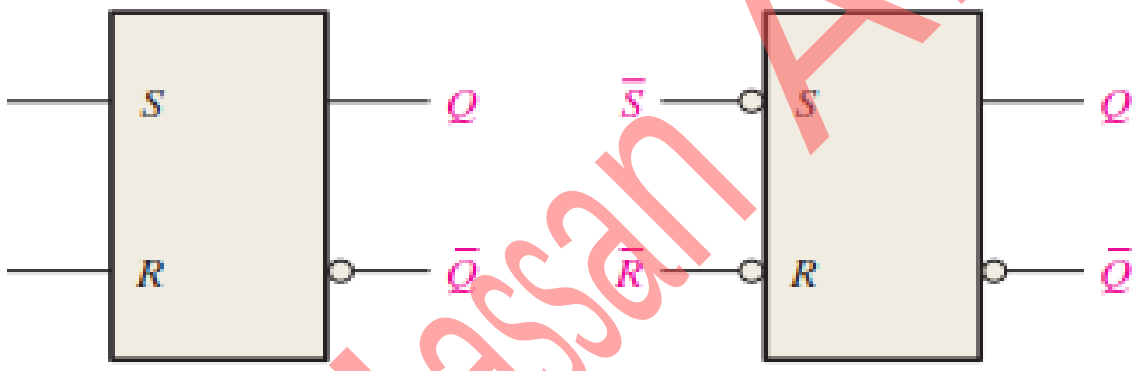
✓ SET means that the *Q* output is HIGH.

✓ RESET means that the *Q* output is LOW.

- Table summarizes the logic operation in **truth table** form.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Logic symbols for both the active-HIGH input and the active-LOW input latches are shown in Fig.



(a) Active-HIGH input S-R latch

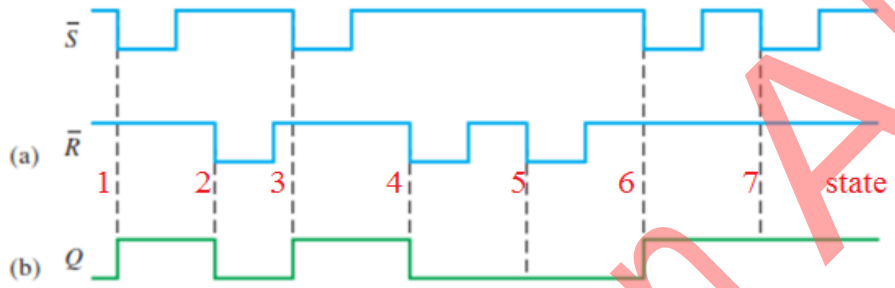
(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

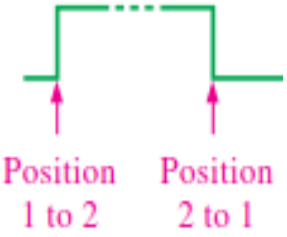
Example 10-1

If the $\overline{S}$ and $\overline{R}$ waveforms in Fig.(a) are applied to the inputs of the active-LOW input $\overline{S}-\overline{R}$ latch, determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

Solution

See Fig.(b).





Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

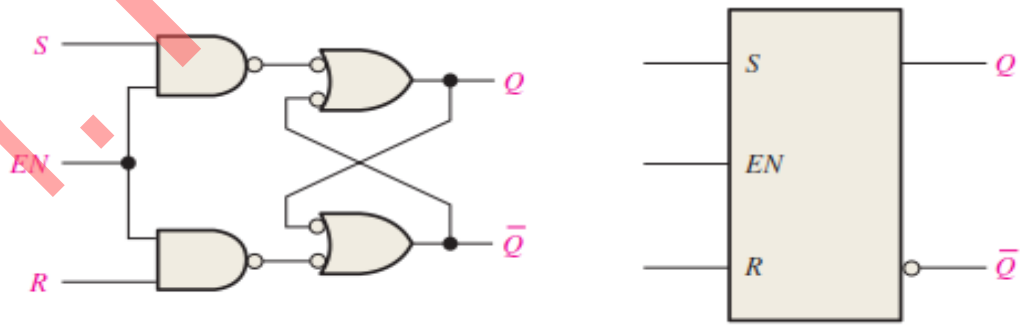
The Q waveform is shown in Fig.(b).

1. When $\overline{S}$ is LOW and $\overline{R}$ is HIGH ➔ latch SET (Q = HIGH).
   - Q output will remain in this state until a LOW is applied to the $\overline{R}$ input.
2. When $\overline{S}$ is HIGH and $\overline{R}$ is LOW , ➔ latch RESET (Q = LOW).
   - The latch remains in the RESET state until a LOW is applied to the $\overline{S}$ input.
3. When $\overline{S}$ is LOW and $\overline{R}$ is HIGH , ➔ latch SET (Q = HIGH).
4. . ➔ latch RESET (Q = LOW)
   - The latch remains in the RESET state until a LOW is applied to the $\overline{S}$ input.
5. Repeated 3. ➔ latch SET (Q = HIGH).

…… Repeated, Repeated……

2. Gated S-R Latch

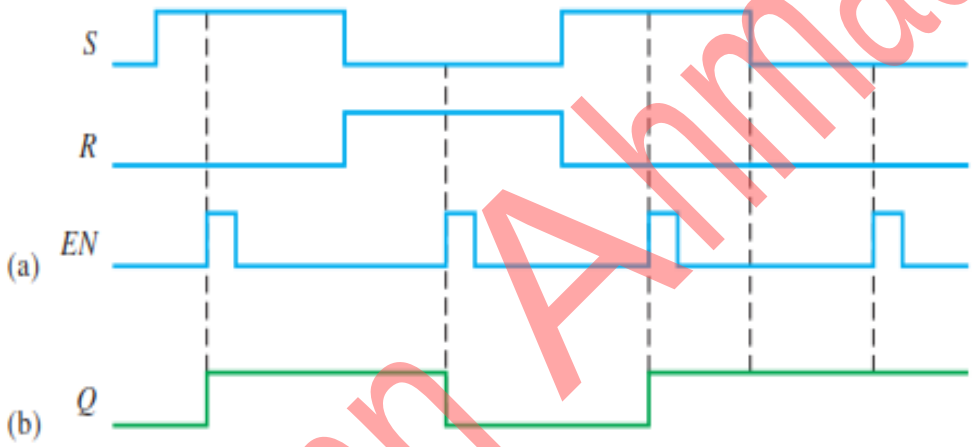
- A gated latch requires an enable input, ***EN*** (***G*** is also used to designate an enable input).
- The logic diagram and logic symbol for a gated *S*-*R* latch are shown in Fig.
- The *S* and *R* inputs control the state to which the latch will go when a HIGH level is applied to the *EN* input.
- The latch will not change until *EN* is HIGH; but as long as it remains HIGH, the output is controlled by the state of the *S* and *R* inputs.
- In this circuit, the **invalid state** occurs when both *S* and *R* are simultaneously (في الوقت ذاته) HIGH and EN is also HIGH.



(a) Logic diagram (b) Logic symbol

Example 10-2

Determine the *Q* output waveform if the inputs shown in Fig.(a) are applied to a **Gated S-R latch** that is initially RESET.



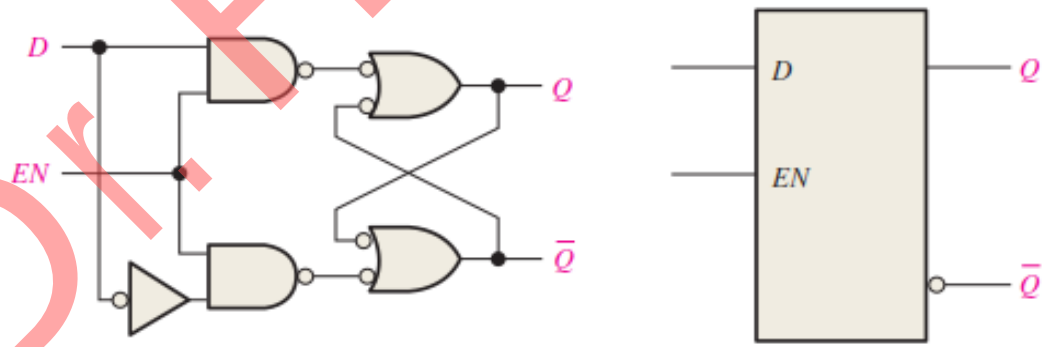
Solution

The *Q* waveform is shown in Fig.(b).

- When *S* is HIGH and *R* is LOW, a HIGH on the EN input sets the latch (HIGH).
- When *S* is LOW and *R* is HIGH, a HIGH on the EN input resets the latch (LOW).
- When both *S* and *R* are LOW, the *Q* output does not change from its present state.

3. Gated D Latch

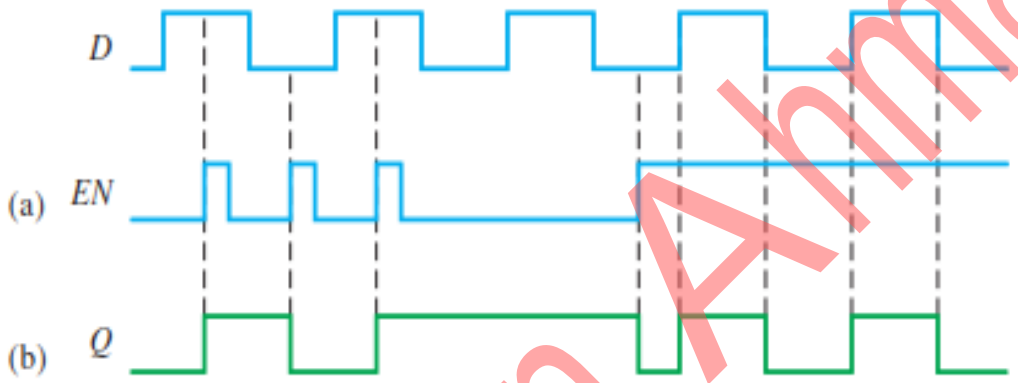
- Another type of Gated latch is called the **D latch**.
  - It differs from the S-R latch because it has only one input in addition to EN.
  - This input is called the ***D* (data) input**.
  - Fig. contains a logic diagram and logic symbol of a D latch.
    - When the *D* input is HIGH and the EN input is HIGH, the latch will SET (HIGH).
    - When the *D* input is LOW and EN is HIGH, the latch will reset (LOW).
    - Stated another way, the output *Q* **follows** the input *D* when EN is HIGH.



(a) Logic diagram (b) Logic symbol

Example 10-3

Determine the *Q* output waveform if the inputs shown in Fig.(a) are applied to a Gated *D* latch, which is initially RESET.



Solution

The *Q* waveform is shown in Fig.(b).

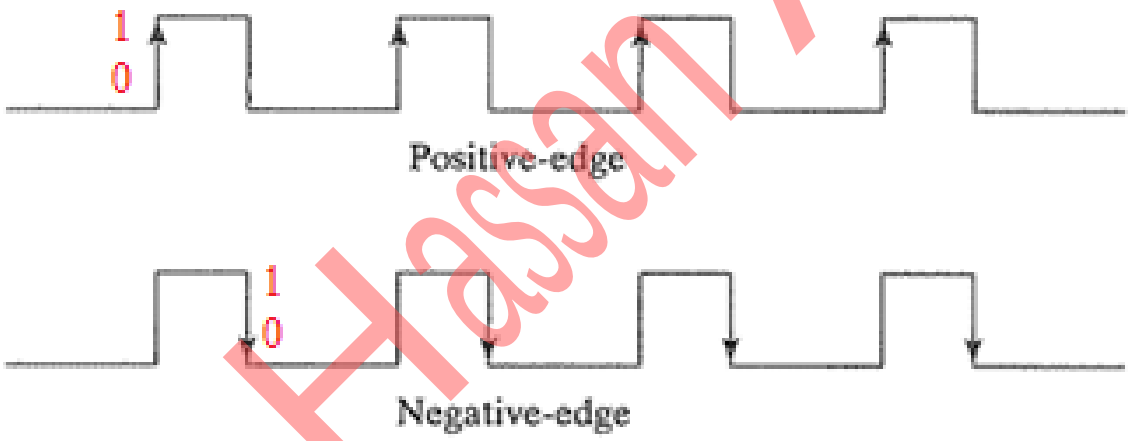
- When *D* is HIGH and EN is HIGH, *Q* goes HIGH.
- When *D* is LOW and EN is HIGH, *Q* goes LOW.
- When EN is LOW, the state of the latch is not affected (يتأثر) by the *D* input.

12-1. Flip-Flops (القلابات)

- **Flip-flops** are synchronous bistable devices, also known as **bistable multivibrators (**هزاز متعدد ثنائي الاستقرار**)**.
  - The term synchronous (متزامن) means that the output changes state only at a specified point (leading or trailing edge (حافة أمامية أو خلفية)) on the triggering input (دخل القدح/الإطلاق) called the **clock** (**CLK**), which is designated as a control input, ***C***; that is, changes in the output occur in synchronization with the clock.
- Flip-flops are edge-triggered or edge-sensitive whereas Gated latches are level-sensitive.

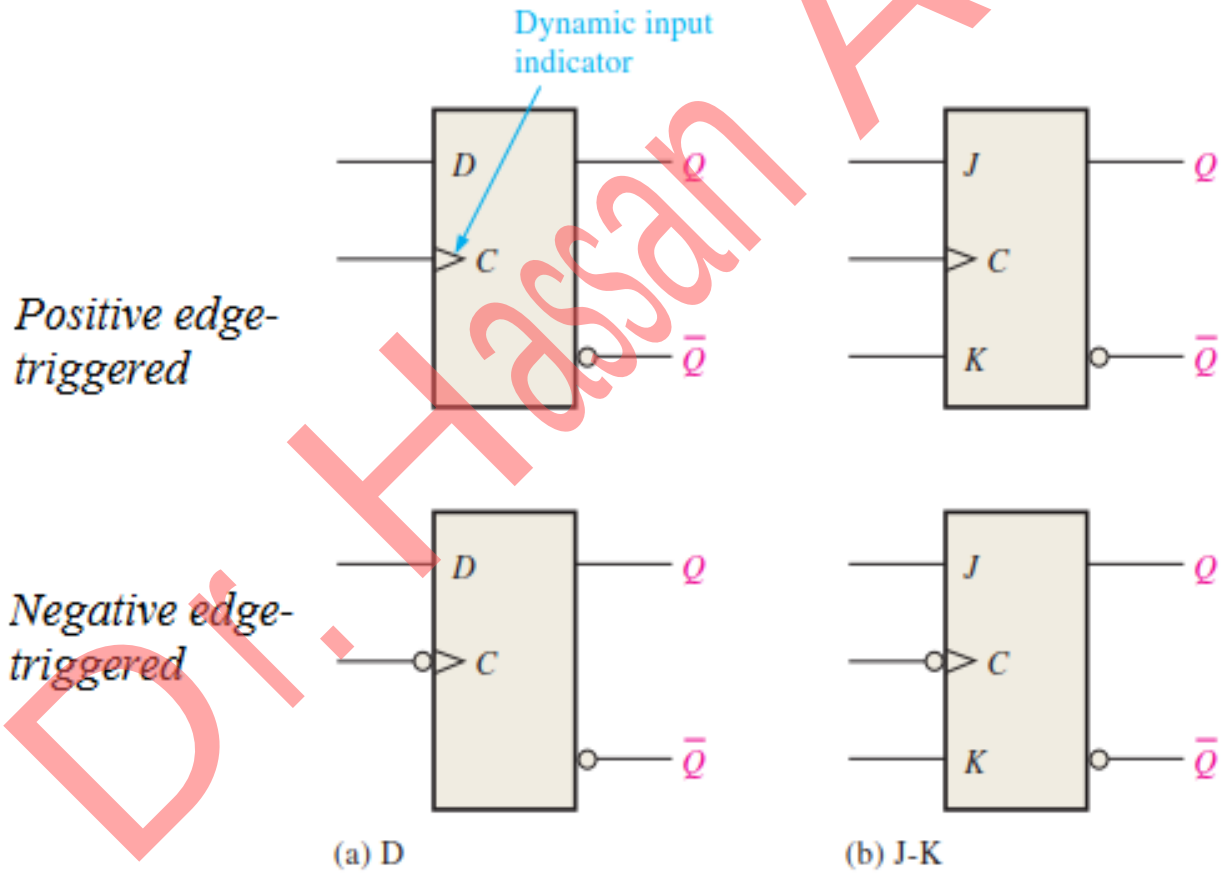
1. Edge-triggered flip-flop

- An edge-triggered flip-flop (قلاب ذو حافة قدح) changes state either at the positive edge (rising edge, الحافة الصاعدة) or at the negative edge (falling edge, الحافة الهابطة) of the clock pulse and is sensitive to its inputs only at this transition of the clock.



Two types of edge-triggered flip-flops are: **D** and **J-K**.

- The logic symbols for these flip-flops are shown in Fig.
  - Notice that each type can be either positive edge-triggered (no bubble at *C* input) or negative edge-triggered (bubble at *C* input).
- The **key** to identifying an edge-triggered flip-flop by its logic symbol is the **small triangle** inside the block at the clock (C) input.
  - This triangle is called the **dynamic input indicator**.



2. The D Flip-Flop

- The *D* input of the D flip-flop is a synchronous input because data on the input are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
- The truth table for positive edge-triggered D flip-flop is

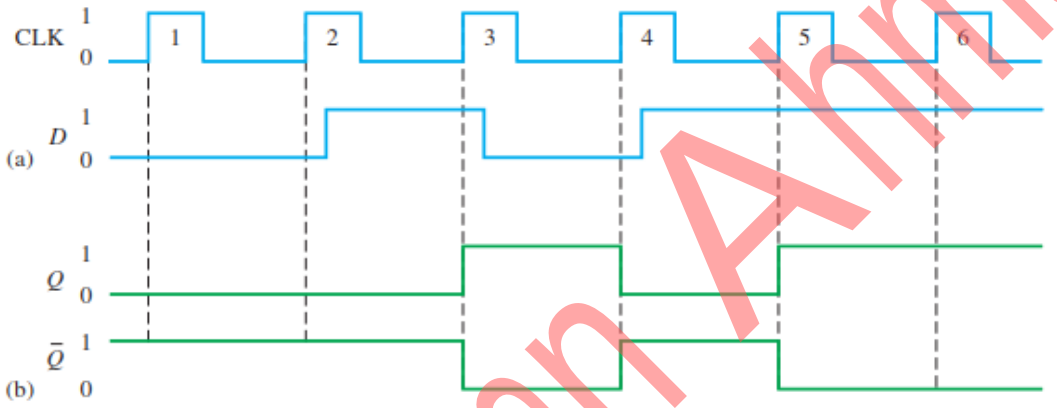
Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

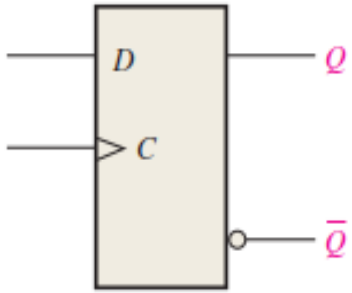
↑ = clock transition LOW to HIGH

- The operation and truth table for a negative edge-triggered D flip-flop are the same as those for a positive edge-triggered device except that the falling edge of the clock pulse is the triggering edge.

Example 10-4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Fig. for the D and CLK inputs in Fig.(a). Assume that the positive edge-triggered flip-flop is initially RESET.





Solution

1. At clock pulse 1, D is LOW, so Q remains LOW (RESET).
2. At clock pulse 2, D is LOW, so Q remains LOW (RESET).
3. At clock pulse 3, D is HIGH, so Q goes HIGH (SET).
4. At clock pulse 4, D is LOW, so Q goes LOW (RESET).
5. At clock pulse 5, D is HIGH, so Q goes HIGH (SET).
6. At clock pulse 6, D is HIGH, so Q remains HIGH (SET).

- ✓ Once Q is determined, $\overline{Q}$ is easily found since it is simply the complement of Q.
- ✓ The resulting waveforms for Q and $\overline{Q}$ are shown in Fig.(b) for the input waveforms in part (a).

3. The J-K Flip-Flop

- The **J** and **K** inputs of the **J-K flip-flop** are synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse.

NOTE: **The flip-flop cannot change state except on the triggering edge of a clock pulse.**

- The **truth table** for a positive edge-triggered flip-flop.

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	*K*	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

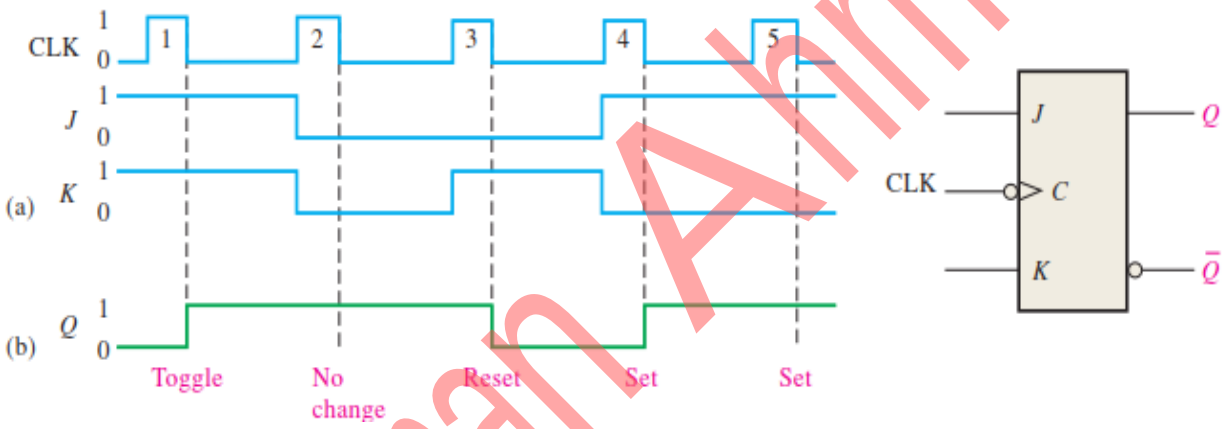
↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition (مستوى الخرج قبل الانتقال إلى الحالة المناسبة للساعة)

- A **J-K** flip-flop connected for **toggle** operation (عملية التبديل) is sometimes called a **T flip-flop**.

Example 10-4

The waveforms in Fig.(a) are applied to the negative edge-triggered *J-K* flip-flop and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.



Solution

Since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the *Q* output will change only on the negative-going edge of the clock pulse.

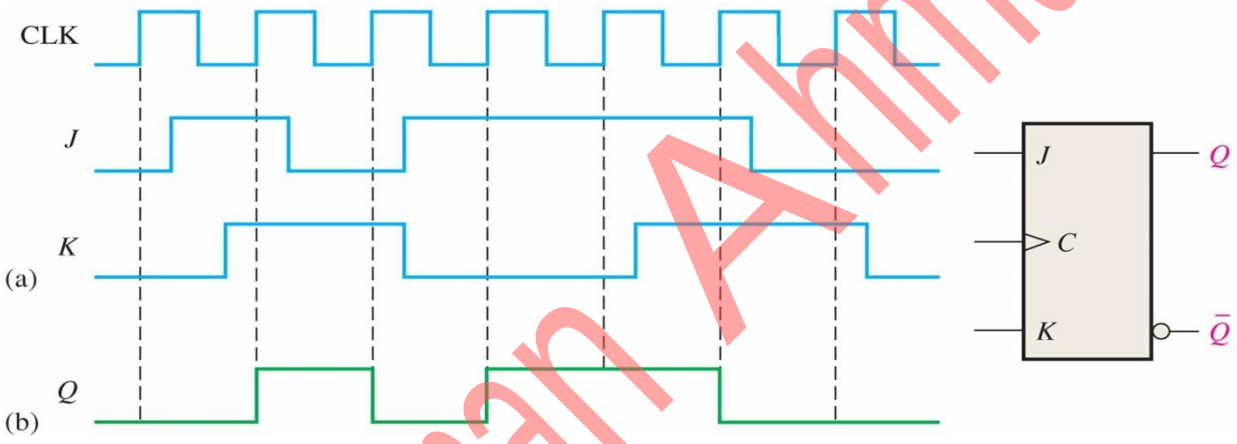
1. At the first clock pulse, both *J* and *K* are HIGH; and because this is a toggle condition, *Q* goes HIGH.
2. At clock pulse 2, a no-change condition exists on the inputs, keeping *Q* at a HIGH level.
3. When clock pulse 3 occurs, *J* is LOW and *K* is HIGH, resulting in a RESET condition; *Q* goes LOW.
4. At clock pulse 4, *J* is HIGH and *K* is LOW, resulting in a SET condition; *Q* goes HIGH.
5. A SET condition still exists on *J* and *K* when clock pulse 5 occurs, so *Q* will remain HIGH.

The resulting *Q* waveform is indicated in Fig.(b).

Example 10-5

The waveforms in Fig.(a) are applied to the positive edge-triggered *J-K* flip-flop and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.

Solution



The *Q* output assumes the state determined by the states of the *J* and *K* inputs at positive-going edge (triggering edge) of the clock pulse.

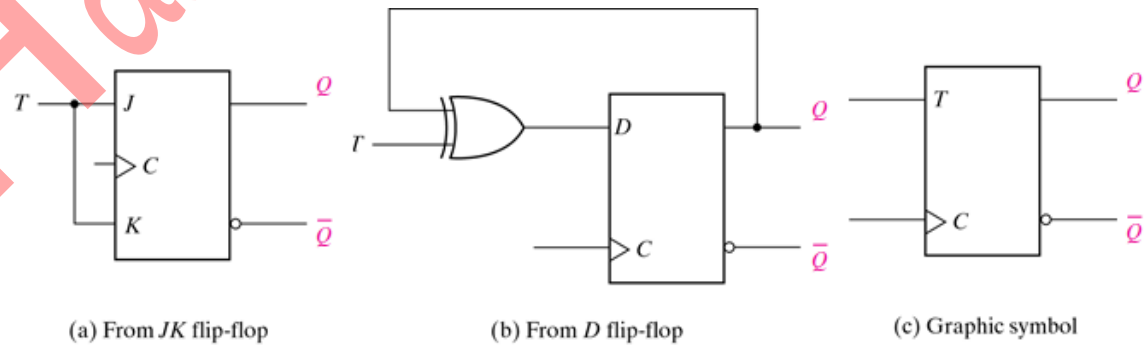
A change in *J* and *K* after triggering edge of the clock has no effect on the output, as shown in Fig.(b).

4. The T Flip-Flop (قلاب التبديل)

- The **T (toggle) flip-flop** is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together, as shown in Fig.(a).
  - When $T = 0$ ($J = K = 0$), a clock edge does not change the output.
  - When $T = 1$ ($J = K = 1$), a clock edge complements the output.
- The complementing flip-flop is useful for designing binary counters.
- The **T flip-flop** can be constructed with a D flip-flop and an exclusive-OR gate as shown in Fig.(b).
  - The expression for the D input is $D = T \oplus Q = T\overline{Q} + \overline{T}Q$
    - When $T = 0$, $D = Q$ and there no change in the output.
    - When $T = 1$, $D = \overline{Q}$ and the output complements.

CLK	T	Output	
		Q	$\overline{Q}$
×	×	0	1
HIGH	0	No change	
HIGH	1	Toggle	
LOW	×	No change	

× -"don't care" state



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

Selected Key Terms

Latch	**A bistable digital circuit used for storing a bit.**
Bistable	Having two stable states. Latches and flip-flops are bistable multivibrators.
Clock	A triggering input of a flip-flop.
D flip-flop	A type of bistable multivibrator in which the output assumes the state of the *D* input on the triggering edge of a clock pulse.
Edge-triggered flip-flop	A type of flip-flop in which the data are entered and appear on the output on the same clock edge.
J-K flip-flop	A type of flip-flop that can operate in the SET, RESET, no-change, and toggle modes.
RESET	The state of a flip-flop or latch when the output is 0; the action of producing a RESET state.
SET	The state of a flip-flop or latch when the output is 1; the action of producing a SET state.
Synchronous	Having a fixed time relationship.
Toggle	The action of a flip-flop when it changes state on each clock pulse.

True/False Quiz

1. A latch has one stable state.
2. A latch is considered to be in the RESET state when the Q output is low.
3. A gated D latch cannot be used to change state.
4. Flip-flops and latches are both bistable devices.
5. An edge-triggered D flip-flop changes state whenever the D input changes.
6. A clock input is necessary for an edge-triggered flip-flop.
7. When both the J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.

1. F 2. T 3. F 4. T 5. F 6. T 7. T

Quiz

1. An active HIGH input S-R latch is formed by the cross-coupling of
   (a) two NOR gates **(b)** two NAND gates **(c)** two OR gates **(d)** two AND gates
2. Which of the following is not true for an active LOW input $\overline{S}-\overline{R}$ latch?
   (a) $\overline{S} = 1, \overline{R} = 1, Q = NC, \overline{Q} = NC$ **(b)** $\overline{S} = 0, \overline{R} = 1, Q = 1, \overline{Q} = 0$
   (c) $\overline{S} = 1, \overline{R} = 0, Q = 1, \overline{Q} = 0$ **(d)** $\overline{S} = 0, \overline{R} = 0, Q = 1, \overline{Q} = 1$
3. For what combinations of the inputs *D* and *EN* will a *D* latch reset?
   (a) D = LOW, *EN* = LOW
   (b) *D* = LOW, *EN* = HIGH
   (c) *D* = HIGH, *EN* = LOW
   (d) *D* = HIGH, *EN* = HIGH
4. A flip-flop changes its state during the
   (a) complete operational cycle
   (b) falling edge of the clock pulse
   (c) rising edge of the clock pulse
   (d) both answers (b) and (c)
5. The purpose of the clock input to a flip-flop is to
   (a) clear the device
   (b) set the device
   (c) always cause the output to change states
   (d) cause the output to assume a state dependent on the controlling (*J-K* or *D*) inputs.

1. (a) 2. (c) 3. (b) 4. (d) 5. (d)

Quiz

6. For an edge-triggered D flip-flop,
- **(a)** a change in the state of the flip-flop can occur only at a clock pulse edge
- **(b)** the state that the flip-flop goes to depends on the *D* input
- **(c)** the output follows the input at each clock pulse
- **(d)** all of these answers

7. A feature that distinguishes the J-K flip-flop from the D flip-flop is the
- **(a)** toggle condition
- **(b)** preset input
- **(c)** type of clock
- **(d)** clear input

8. A flip-flop is SET when
- **(a)** $J = 0, K = 0$
- **(b)** $J = 0, K = 1$
- **(c)** $J = 1, K = 0$
- **(d)** $J = 1, K = 1$

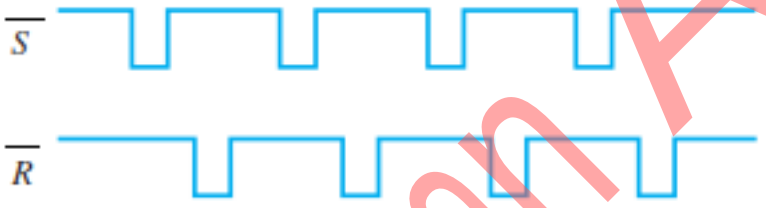
9. A J-K flip-flop with $J = 1$ and $K = 1$ has a 10 kHz clock input. The Q output is
- **(a)** constantly HIGH
- **(b)** constantly LOW
- **(c)** a 10 kHz square wave
- **(d)** a 5 kHz square wave

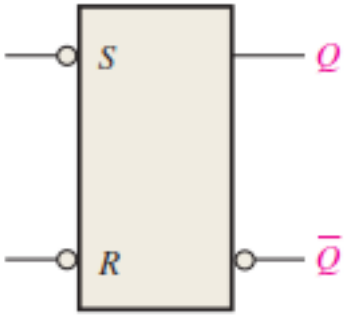
6. (d) **7.** (a) **8.** (c) **9.** (d)

Problems & Solutions

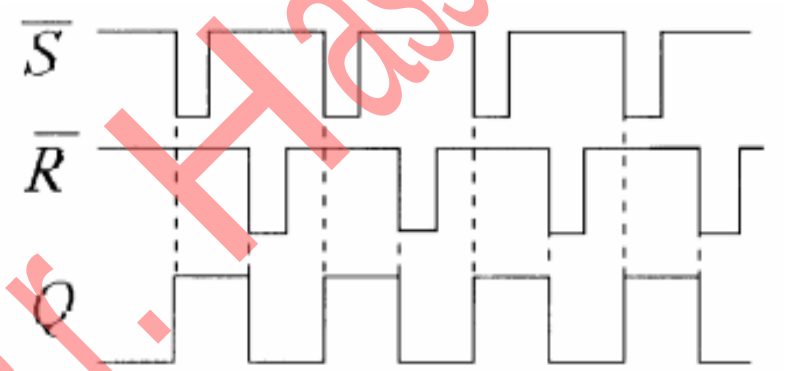
Prob. 7-1

If the waveforms in Figure are applied to an active-LOW S-R latch, draw the resulting *Q* output waveform in relation to the inputs. Assume that *Q* starts LOW.



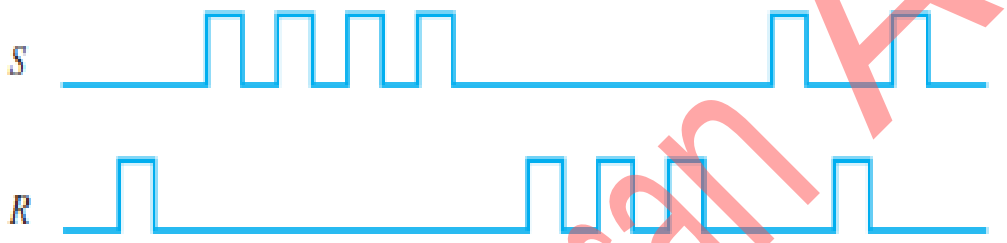


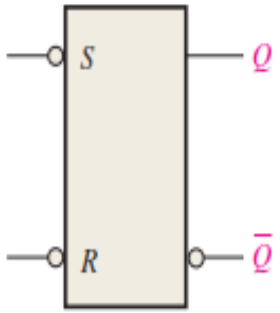
Sol.



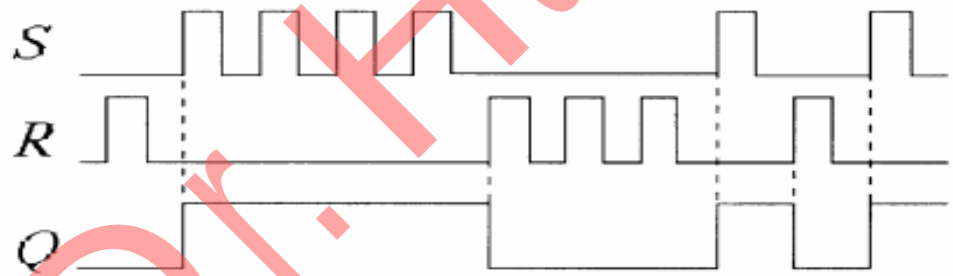
Prob. 7-2

If the waveforms in Figure are applied to an active-HIGH S-R latch, draw the resulting *Q* output waveform in relation to the inputs. Assume that *Q* starts LOW.



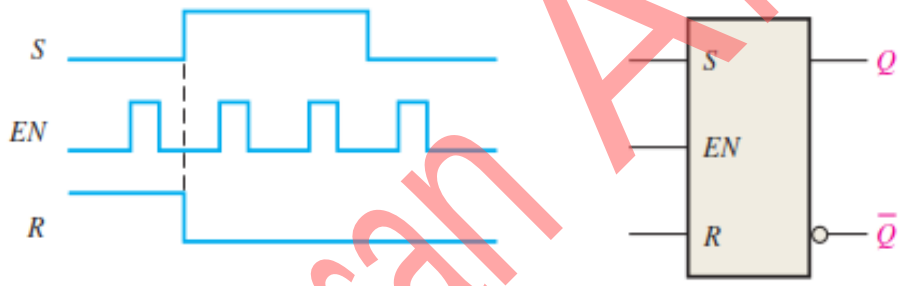


Sol.

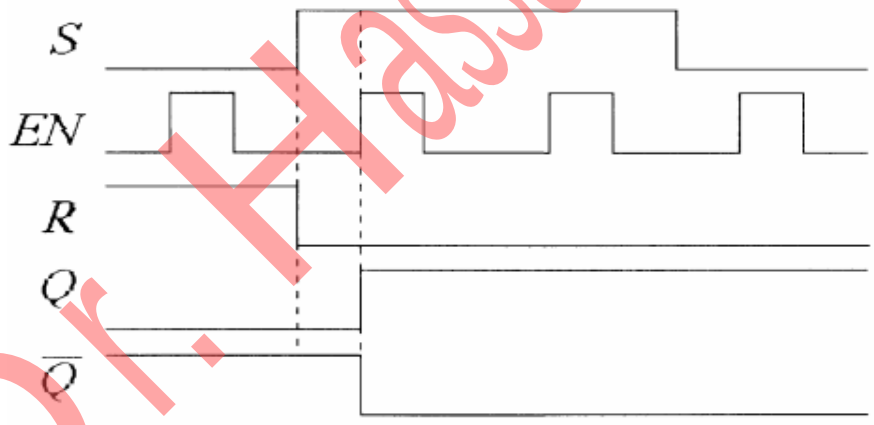


Prob. 7-3

For a gated S-R latch, determine the Q and $\overline{Q}$ outputs for the inputs in Figure. Show them in proper relation to the enable input. Assume that Q starts LOW.

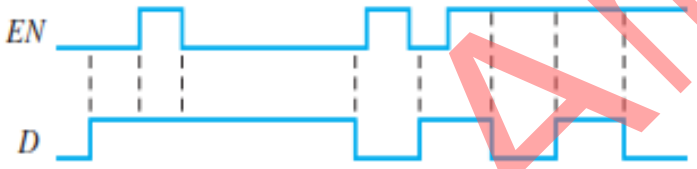


Sol.

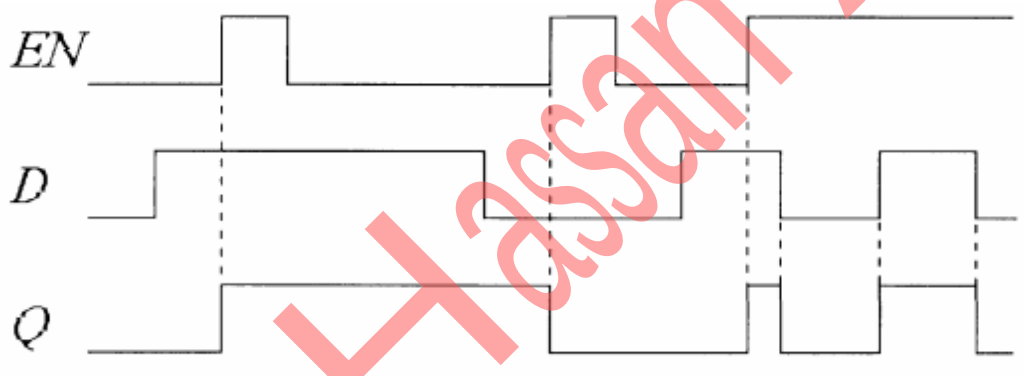


Prob. 7-4

For a gated D latch, the waveforms shown in Figure are observed on its inputs. Draw the timing diagram showing the output waveform you would expect to see at *Q* if the latch is initially RESET.

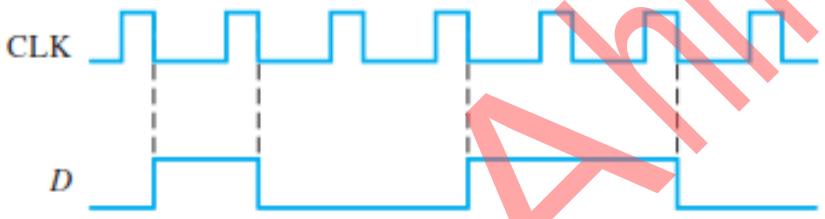


Sol.

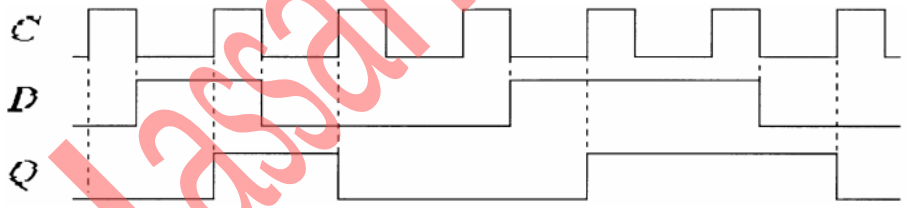


Prob. 7-5

Draw the *Q* output relative to the clock for a D flip-flop with the inputs as shown in Figure. Assume positive edge-triggering and *Q* initially LOW.

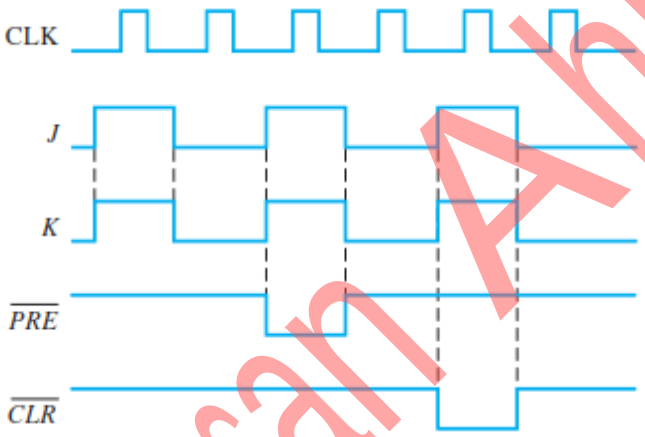


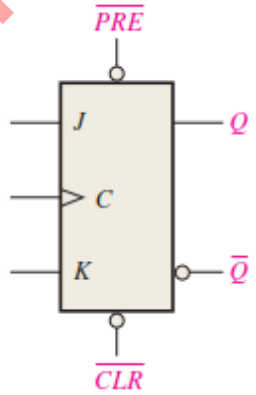
Sol.



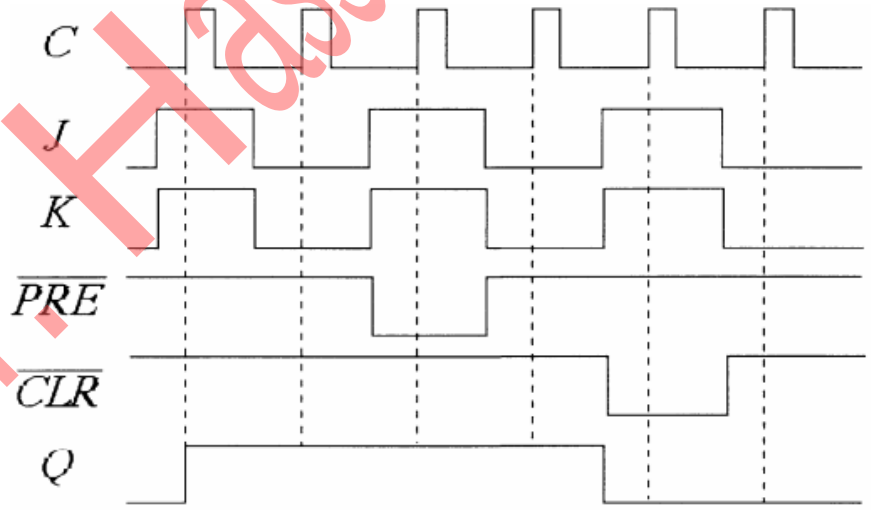
Prob. 7-6

Determine the *Q* waveform relative to the clock if the signals shown in Figure are applied to the inputs of the J-K flip-flop. Assume that *Q* is initially LOW.



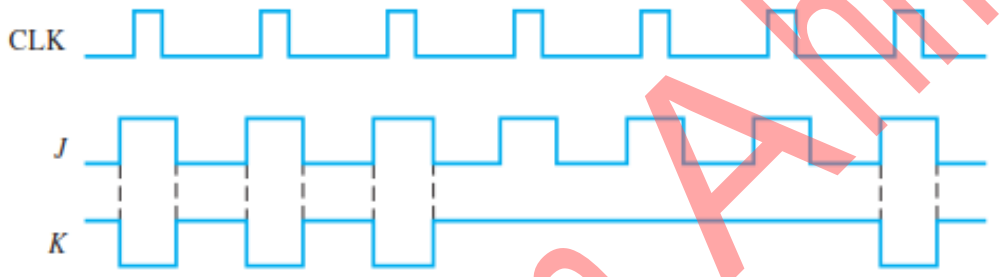


Sol.

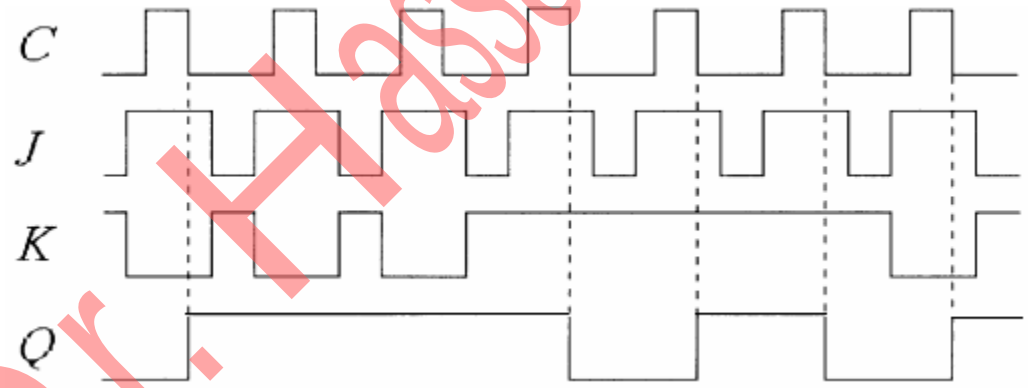


Prob. 7-7

For a negative edge-triggered J-K flip-flop with the inputs in Figure, develop the *Q* output waveform relative to the clock. Assume that *Q* is initially LOW.



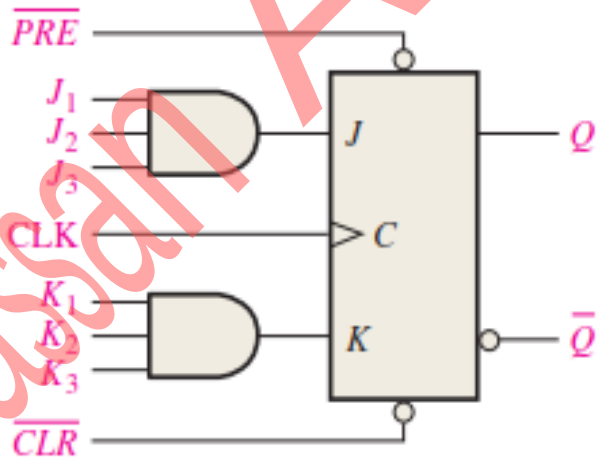
Sol.



Prob. 7-8 The following serial data are applied to the flip-flop through the AND gates as indicated in Figure.

Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Right-most bits are applied first.

J_1: 1 0 1 0 0 1 1; J_2: 0 1 1 1 0 1 0; J_3: 1 1 1 1 0 0 0; K_1: 0 0 0 1 1 1 0; K_2: 1 1 0 1 1 0 0;
K_3: 1 0 1 0 1 0 1



Sol.

J: 0010000
K: 0000100
Q: 0011000

The end of Lecture_10, chapter 7